REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The Office Action dated July 14, 2008, has been received and its contents carefully reviewed.

Claims 1-14 are rejected by the Examiner. With this response, claims 1, 7 and 13 are amended. No new matter has been added. Claims 1-14 remain pending in this application.

In the Office Action, claims 1, 3, 4, and 6-14 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,535,194 to Hanano (hereinafter "Hanano"). Claims 2 and 5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hanano in view of U.S. Patent No. 4,097,128 to Matsumoto (hereinafter "Matsumoto").

The rejection of claims 1, 3, 4, and 6-14 is respectfully traversed and reconsideration is requested.

Claims 1, 3, 4, and 6-12 are allowable over the cited references in that each of these claims recites a combination of elements including, for example, "a light shutter on the liquid crystal display panel operable to transmit and shut off a light emitted from the liquid crystal display panel during every field period" and "wherein every field period is initiated upon a first transition of a gate signal from a low voltage signal to a high voltage signal to apply image data to the pixel and is terminated upon a next transition of the gate signal from a low voltage signal to a high voltage signal to apply image data to the pixel, and wherein the light shutter is opened at a first transition of the gate signal such that the transmittance of light shutter is substantially zero before opening and closed after the first transition of the gate signal and before the next transition of the gate signal per every frame period for each pixel such that the transmittance of light shutter is substantially zero after closing." Hanano does not teach or suggest at least this feature of the claimed invention.

In rejecting claims 1 and 7, the Examiner refers to Fig. 5a as teaching Even and Odd halves make up a single frame image. The Examiner states that Fig. 5a of Hanano teaches "wherein every field period is initiated upon a first transition of a gate signal from a low voltage signal to a high voltage signal to supply data to apply image data to the pixels and is terminated upon a next transition of the gate signal from a low voltage signal to a high voltage signal to

apply image data to the pixels, wherein every field period corresponds to only one image data value, and wherein the light shutter is opened at a first transition of the gate signal and closed after the first transition of the gate signal and before the next transition of the gate signal per every frame period." But, Fig. 5a of Hanano does not teach or suggest at least this feature of the claimed invention.

Hanano discloses a system using a shutter to either make an LCD display look like it is higher resolution or to produce stereo images to provide parallax to create 3D images. See col. 6, lines 29-44 and col. 17, lines 36-39. These two images are referred to as even and odd images. The even and odd frames are created by sampling the image signal separated in time corresponding to the extent of image shift. See col. 2, lines 38-41.

In the Office Action, the Examiner states Fig. 5a of Hanano has "Even and Odd halves [that] make up a single frame image which is a single image data value." This is not the case, as the even and odd frames contain different data by sampling the image signal at two different times. When the Examiner combines the even and odd frames to make up a single frame, there are two different image data values rather than the claimed single image data value. So in reality, the even and odd frames are completely separate frames. So in Fig. 5a, the time where the shutter is open spans both the even and odd frames. This is especially true in Figs. 3, 4, 7, and 8, where the shutter open time spans the transition from a even to an odd field for a given pixel. Hence, the light shutter is not closed before the next transition of the gate signal per every frame period as claimed. Further, in Fig. 5a, the transmittance of the light shutter is substantially zero before the first transistion of the gate signal and after the next transistion of the gate signal. This is shown where the tranmitance curve is great than zero outside of the EVEN FIELD.

Also, Hanano teaches that "the field detecting circuit 32 generates a field synchronizing signal as shown in FIG. 4c according to the synchronizing signal (corresponding to the gate signal of the claimed invention) from the image display control circuit 11, the delayed signal generating circuits 33 and 34 delay the field synchronizing signal by times $\tau 1$ and $\tau 2$, respectively as shown in FIGs. 4d and 4e, according to the response characteristic of the TN shutter 2 itself, and the TN shutter drive signal generating circuit 35 generates a TN shutter drive signal (FIG. 4f) by using the first delayed field synchronizing signal (FIG. 4d) as a set signal and the second delayed field synchronizing signal (FIG. 4e) as a reset sgnal." In Hanano, the light

shutter is not opened at a transition of the first field synchronizing signal from a low voltage signal to a high voltage signal, but is rather delayed by a time after the transition of the first field synchronizing signal. This can be seen in the various figures of Hanano where a transition of the first field synchronizing signal from a low voltage signal to a high voltage signal does not correspond to when the shutter is opened.

Fig 5a of Hanano explains that a contrast improvement of about 53% can be obtained compared to the prior art, when the time **tb** and the duty ratio **df** are set as the formulas (7) and (8), and the delay times **τ1** and **τ2** are controlled as the formulas (9) and (10). So Hanano sets out to have a delay between the shutter opening and the transition of the first field synchronizing signal from a low voltage signal to a high voltage signal.

Therefore, Hanano does not teach these features of claims 1 and 7. Accordingly, Applicant submits that claims 1 and 7, and claims 3, 4, 6, 8-12 depending upon claims 1 and 7, are allowable over Hanano for at least this reason.

Claims 13 and 14 are allowable over the cited references in that each of these claims recites a method of driving a liquid crystal display, having a combination of features including, for example, "opening the light shutter at a first transition of the gate signal from a low voltage signal to a high voltage signal such that the transmittance of light shutter is substantially zero before opening; and closing the light shutter after the first transition of the gate signal and before a next transition of the gate signal from a low voltage signal to a high voltage signal per every frame period for each pixel such that the transmittance of light shutter is substantially zero after closing." In the Office Action, the Examiner rejects claim 13 using the same rationale given for claim 1. Applicant's submits that Hanano does not teach or suggest at least the above identified features of claims 13 and 14 for at least the reasons given above for claim 1. Accordingly, Applicant submits that claims 13 and 14 are allowable over Hanano.

The rejection of claims 2 and 5 is respectfully traversed. As discussed above with respect to claims 1, 3, 4, and 6-14, Hanano fails to teach the features discussed above. Matsumoto fails to cure this deficiency of Hanano. Accordingly, Applicant submits that claims 2 and 5 are allowable over Hanano and Matsumoto.

Applicants believe the foregoing amendment and remarks place the application in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911.

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Respectfully submitted,

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